

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("6807520").PN.	USPAT; USOCR	OR	OFF	2006/10/04 08:37
L2	6	((("5555201") or ("5838947") or ("6108494") or ("6339836") or ("6446239") or ("6449761"))).PN.	USPAT; USOCR	OR	OFF	2006/10/04 08:47
L3	4745	716/3 716/5 716/6 716/7 716/8 716/9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/04 08:47
L4	93	L3 and (circuit and hierarchical\$2). ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/04 08:48
L5	15	L3 and (circuit and hierarchical\$2 and (simulat\$4 or verif\$6)).ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/04 08:49
S1	0	(circuit same (simulat\$4 or verif\$6)) and (hierarchical same branch same (leaf or leaves)) and netlist and ( (static same database) and (dynamic same database))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/23 18:05
S2	9	(circuit same (simulat\$4 or verif\$6)) and (hierarchical same branch same (leaf or leaves)) and netlist	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/23 18:07
S3	53	(circuit same (simulat\$4 or verif\$6)) and (hierarchical same (leaf or leaves)) and netlist	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/24 11:27
S4	39	"5446676"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/24 09:41

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S5	2	"5446676".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/24 09:41
S6	4	"553008".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/24 09:42
S7	2	"5553008".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/24 09:42
S8	6	((("5555201") or ("5838947") or ("6108494") or ("6339836") or ("6446239") or ("6449761"))).PN.	USPAT; USOCR	OR	OFF	2006/03/24 10:41
S9	2	"6807520".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/02 14:16
S10	6	"808339".ap.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/24 11:27
S11	958	703/14.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/24 11:27
S12	8	S11 and (circuit same (simulat\$4 or verif\$6)) and (hierarchical same (leaf or leaves)) and netlist	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/24 11:27

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S13	2	"6026226".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/24 15:22
S14	2	"6339836".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/24 15:22
S15	6	("5555201"   "5838947"   "6108494"   "6339836"   "6446239"   "6449761").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/03/24 15:41
S16	2	"6629044".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/02 14:36
S17	2	"5608328".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/02 14:36
S18	161	(circuit and hierarchical and (simulat\$4 or verif\$6)).ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/03 14:19
S19	20	S18 and static and dynamic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/04 07:50
S20	181	(hierarchical\$2 and circuit and (simulat\$4 or verif\$6)).ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/04 07:51

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S21	8	S20 and branch and (leaf or leaves)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/04 07:55
S22	1075	703/14.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/04 07:55
S23	15	S22 and (circuit and hierarchical\$2).ab.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/10/04 08:47



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Y Wong - Proceedings of the 22nd ACM/IEEE conference on Design ... , 1985 - portal.acm.org  
... signalnet graph) format as used by the **simulator** program esim[1] ... the CIF description  
and the specification of the **circuit** into **hierarchical** signalnet graphs ...

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TOC View - Memory Technology, Design, and Testing, 2005. MTD 2005. ... , 2005 - [ieeexplore.ieee.org](#)  
... from a DSPF file where stitched into the **hierarchical** LVS netlist. ... On another 90nm  
SRAM **circuit** the importance of high accuracy postlayout **simulation** can be ...

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LG Jones, DT Blaauw, SSD Technol, M Inc, TX Austin - Computer-Aided Design of Integrated Circuits and  
Systems, ... , 1994 - [ieeexplore.ieee.org](#)

... the cache-based **simulation** method presented in the previous ... n = 6 (a 64-bit AND **circuit**)  
the cache ... exponential in the size of the **hierarchical** description, it ...

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### [Exploiting hierarchy in a cache-based switch-level simulator](#)

LG Jones - Design Automation, 1992. Proceedings.[3rd] European ... , 1992 - [ieeexplore.ieee.org](#)

... If the cached **simulation** method presented in the ... Schematic hierarchy of a 2"-input  
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S Sangameswaran, S Yamauchi - Architecture, Circuits and Implementation of SOC's, 2005. ... , 2005 -  
[ieeexplore.ieee.org](#)

... the timing-domain behavior of the **circuit** and speeding ... partially address this problem  
a **hierarchical** netlist is ... Parasitic RC **simulation** needs a large amount of ...

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### [Hierarchical mixed simulation for intelligent interfaces of microsystems - group of 4 »](#)

T Niculiu, S Cotofana, A Manolescu - Semiconductor Conference, 1999. CAS'99 Proceedings. 1999 ... , 1999 -  
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... The modularity that characterizes **hierarchical simulation** can be ... Dynamics, **circuit**  
theory, hydrodynamics, thermodynamics ... a direct physical **simulation** of heat ...

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KA Gallivan, BA Marsolf, HAG Wijshoff - Proceedings of the 8th international conference on ... , 1994 -  
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... tational fluid dynamics, **circuit simulation**, and structural mechanics ... **dynamic**  
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 P Mazumder - IEEE Transactions on Computers, 1993 - doi.ieeecomputersociety.org  
 ... The Monte Carlo **simulation** done by Sai-Halas et al. ... Encoding and decoding **circuit**  
 for the code should not ... Usually in a **hierarchical** memory system, with  $N = kn$  ...  
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#### [High Capacity and Automatic Functional Extraction Tool for Industrial VLSI Circuit Designs](#) - group of 9 »

S Novakovsky, S Shyman, Z Hanna - Proceedings of the 2002 IEEE/ACM international conference on ..., 2002 - doi.ieeecomputersociety.org  
 ... delay modeling for formal verification and **simulation** needs. ... **Hierarchical** extraction in FEV-Extract is attempted for each sub **circuit** that contains ...  
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PA Fishwick - IIE Transactions, 1998 - Springer  
 ... constraint graph is an analog electrical **circuit** or a ... set of hi- erarchies which specify two **hierarchical** relations among ... **Simulation** is made more comprehensible ...  
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B Mathew, JA Wehbeh, DG Saab - Urbana - pdf.aiaa.org  
 ... only restrictions are that the two **hierarchical** designs represent ... the speci- fication and synthesized RTL **circuit**. ... the sequence of symbolic **simulation** and back ...  
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R Barth, B Serlet - Design Automation Conference, 1988. Proceedings., 25th ACM/ ..., 1988 - ieeexplore.ieee.org  
 ... In a lumped element **circuit** abstraction of a technology, the primitives ... the **simulator**. ...  
 Some tools, such as simulators, flatten the **hierarchical** net list into a ...  
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#### [Mighty: a rip-up and reroute detailed router](#) - group of 3 »

H Shin, A Sangiovanni-Vincentelli - International Conference on Computer-aided Design, 1986 - acm.org  
 ... M. and Pelavin, R. "Hierarchical Channel Router ... Although no fault **simulation** is needed,  
 analysis ... pseudorandom testing requires the **circuit** detectability profile ...  
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... tational fluid dynamics, **circuit simulation**, and structural mechanics ... **dynamic** identification and application of parallel ... **Hierarchical Method**, and the level set ...

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JE Harlow, F Brglez - Formal Methods in Computer-Aided Design (FMCAD'98) - Springer

... Treat- Initial **Dynamic** ment Ordering Ordering (in VIS [14]) ... ways: (1) as results of a nominal **simulation** applied to inputs of the reference **circuit** only and ...

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[Analog HDL representation of active filters and noise effects](#)

T Niculiu, K Hofmann, S Dobre, N Cosmin, A ... - Semiconductor Conference, 1995.

CAS'95 Proceedings., 1995 ... , 1995 - [ieeexplore.ieee.org](#)

... knowledge as functions (generic, **hierarchical behavior**), typifying ... data+operations),

managing **simulation** knowledge as ... electrodynamics and **circuit theory** can ...

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T Niculiu, S Cotofana - ... Simulation Multiconference on Modelling and Simulation

2002 ... , 2002 - [fasolt.opentlib.org](#)

... The **hierarchical principle**, applied to knowledge ... Dynamics, **circuit theory**, hydrodynamics,

thermodynamics, electrodynamics ... a direct physical **simulation** of heat ...

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[Evaluation and Improvements of Boolean Comparison Method Based on Binary Decision Diagrams - group of 3 »](#)

M Fujita, H Fujisawa, N Kawato - Proc. of the International Conference on Computer Aided ... , 1988 - [sigda.org](#)

... Burstein and R. Pelavin **Hierarchical wire routing** ... a multirate, event driven **circuit simulator** suitable for ... incorporates both **static** and **dynamic** partitioning of ...

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[Verity-a formal verification program for custom CMOS circuits - group of 5](#)

»

A Kuehlmann, A Srinivasan, DP LaPolin - IBM Journal of Research and Development, 1995 - [cadence.com](#)

... ANAMOS is applied primarily for gate-level **simulation** of transistor ... The basic idea of **hierarchical verification** is to reduce the **circuit complexity** by ...

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